



FPGA Configurator

FC512

Interconnect Systems, Inc.
www.isipkg.com

DATA SHEET

FEATURES

- Ultra-Compact Configuration Solution
- 512Mbit Flash + Controller
- Supports up to 32-bit wide Fast Passive Parallel (FPP) configuration bus
- Complies with 100ms PCIe spec for large FPGAs including Altera Stratix V 5SGXA7, 5SGXB6, 5SGTC7 and 5SGSD8 using 32b FPP
- JTAG interface for programming internal Flash
- 13x13mm 216-ball BGA Package
- Available with either lead-free (RoHS 6/6) or eutectic Sn/Pb (RoHS 5/6) solder balls
- Future feature: Unused flash memory can be used for non-volatile user data space

DESCRIPTION

The FC512 is a single device configuration solution that includes 512Mbits of FLASH storage for configuration data and a controller in a compact 216-ball, 0.8mm pitch BGA package.

APPLICATIONS

Fastest Configuration Time Provides:

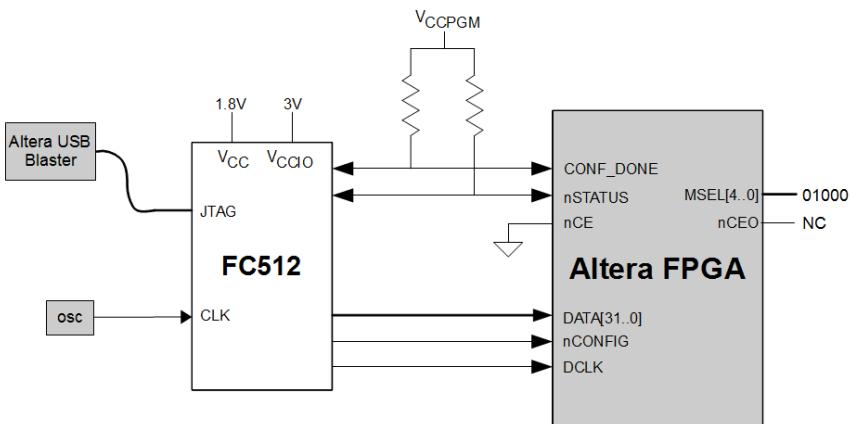
Fast system-on time for embedded applications

Comply with PCIe 100ms spec for large FPGAs including 5SGXA7, 5SGXB6, 5SGTC7 and 5SGSD8

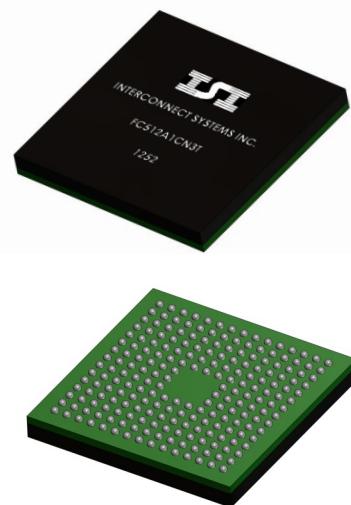
Minimize PCB Area:

13x13 BGA package provides complete configuration solution in 1/4 the area of a typical CPLD + Flash

TYPICAL APPLICATION

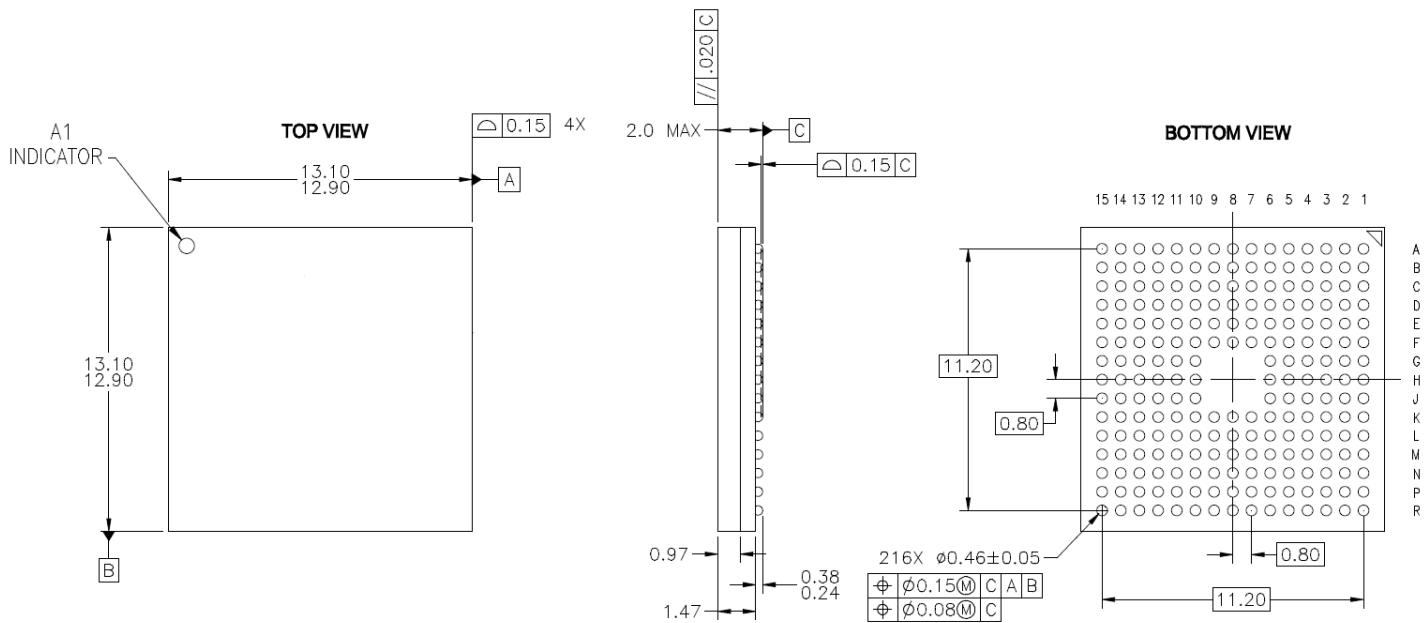


216-Ball BGA Package

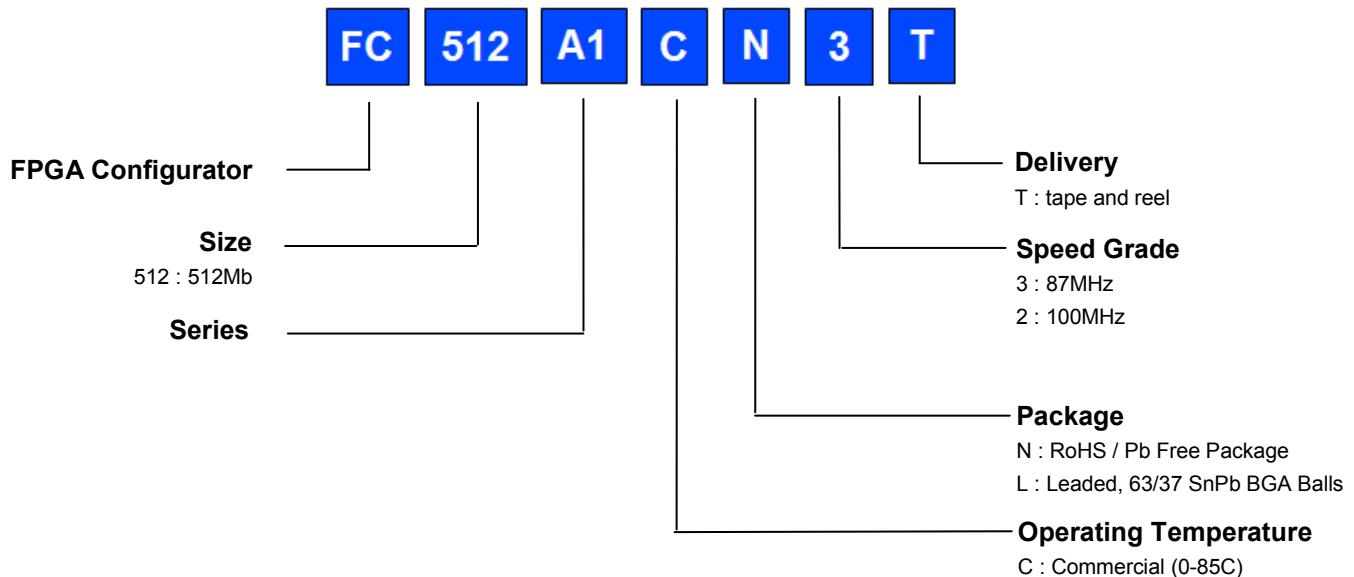


Actual Size (13mm x 13mm)

PACKAGE OUTLINE



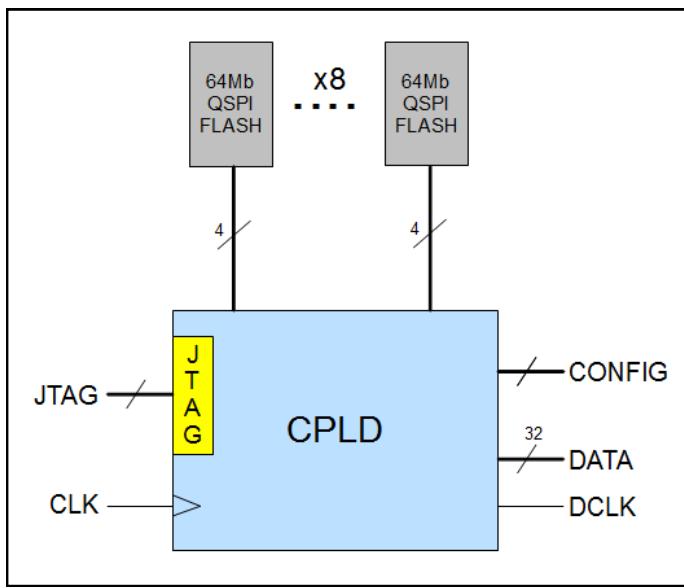
ORDERING INFORMATION



Contact ISI for information on planned speed grade and operating temperature options

Table 1 : Ball Assignments

Name	Ball	Type	Description
CLK	R8	input	Device clock
JTCK	C2	input	
JTMS	C4	input	
JTDI	B2	input	
JTDO	C3	output	
CONF_DONE	F15	input	
nSTATUS	H15	input	
nCONFIG	B1	output	
CONF_RST#	J1	input	PFL Reset
DCLK	K14	output	Configuration clock
D0	E1	output	Configuration data bus
D1	A14		
D2	A9		
D3	K1		
D4	J2		
D5	L1		
D6	A10		
D7	A3		
D8	F1		
D9	E2		
D10	A2		
D11	H2		
D12	G1		
D13	L15		
D14	A11		
D15	F2		
D16	A4		
D17	K2		
D18	J14		
D19	B13		
D20	L14		
D21	M1		
D22	D2		
D23	A5		
D24	A12		
D25	J15		
D26	G15		
D27	B7		
D28	B8		
D29	B11		
D30	A13		
D31	A6		
VCC	E6, E9, F11, G5, J11, K5, L7, L10	power	Core Power
VCCIO	D5, D11, E4, E7, E10, E12, F5, F6, F8, F10, G11, H6, H10, J5, K6, K8, K10, K11, L4, L6, L9, L12, M5, M11	power	I/O Power
GND	A1, A15, B3, B14, D6, D7, D9, D10, E5, E8, E11, F4, F7, F9, F12, F14, G4, G6, G10, G14, H4, H5, H11, J4, J6, J10, J12, K4, K7, K9, K12, L5, L8, L11, M6, M7, M9, M10, P2, P14, R1, R15		
N/C	A7, A8, B4, B5, B6, B9, B10, B12, B15, C1, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, D1, D3, D4, D8, D12, D13, D14, D15, E3, E13, E14, E15, F3, F13, G2, G3, G12, G13, H1, H3, H12, H13, H14, J3, J13, K3, K13, K15, L2, L3, L13, M2, M3, M4, M8, M12, M13, M14, M15, N1, N2, N3, N4, N5, N6, N7, N8, N9, N10, N11, N12, N13, N14, N15, P1, P3, P4, P5, P6, P7, P8, P9, P10, P11, P12, P13, P15, R2, R3, R4, R5, R6, R7, R9, R10, R11, R12, R13, R14	reserved	Leave Unconnected

**Figure 1. Block Diagram**

APPLICATION INFORMATION

Figure 1 shows the internals of the FPGA Configurator. The Altera MAX-series CPLD and NOR QSPI Flash are integrated in a 13mm x 13mm BGA package.

The CPLD contains the Altera PFL megafunction for user programming of the Flash through the JTAG interface and configuration of the Altera FPGA. Refer to the Altera Parallel Flash Loader Megafunction User Guide for more information.

The FC512 operates in Fast Passive Parallel mode with a 32-bit wide configuration data bus (FPP x32) and an MSEL setting of 01000 (decompression and security features disabled, fast POR).

Table 2 lists the resulting configuration time for a range of Altera FPGAs when operating the Configurator at the maximum frequency (see AC Characteristics section). The time is calculated using the following formula:

$$\text{.rbf Size} / 32 \times (1/\text{DCLK})$$

Table 2 : Configuration Time

Device	rbf size (bits)	Configuration ¹ Time (ms)
Stratix V GX		
5SGXA3	213,798,720	77
5SGXA4	213,798,720	77
5SGXA5	269,978,848	97
5SGXA7	269,978,848	97
5SGXA9	387,394,048	139
5SGXAB	387,394,048	139
5SGXB5	270,528,480	97
5SGXB6	270,528,480	97
5SGXB9	387,394,048	139
5SGXBB	387,394,048	139
Stratix V GT		
5SGTC5	269,978,848	97
5SGTC7	269,978,848	97
Stratix V GS		
5SGSD3	93,080,448	33
5SGSD4	209,935,224	75
5SGSD5	209,935,224	75
5SGSD6	266,798,896	96
5SGSD8	266,798,896	96
Stratix V E		
5SEE9	387,394,048	139
5SEEB	387,394,048	139
Arria V GZ		
E1	137,598,720	49
E3	137,598,720	49
E5	213,798,720	77
E7	213,798,720	77

¹ DCLK = 87MHz

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	MIN	MAX	UNITS
V_{CC}	Core supply voltage	-0.5	2.4	V
V_{CCIO}	I/O supply voltage	-0.5	4.0	V
V_I	Input voltage	-0.5	4.0	V

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	MIN	TYP	MAX	UNITS
V_{CC}		1.71	1.80	1.89	V
V_{CCIO}		2.85		3.46	V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNITS
V_{IH}	High-level input voltage		1.7	4.0		V
V_{IL}	Low-level input voltage		-0.5	0.8		V
V_{OH}	High-level output voltage	$V_{CCIO} = 3.0V, I_{OH} = -0.1mA$	VCCIO-0.2			V
V_{OL}	Low-level output voltage	$V_{CCIO} = 3.0V, I_{OL} = 0.1mA$		0.2		V
I_{CC}	Operating current, V_{CC}	$V_{CC} = 1.8V$		12	80	mA
I_{CCIO}	Operating current, V_{CCIO}	$V_{CCIO} = 3.0V$		3	175	mA

Notes :

Max current applies to configuration time. Typ current applies to idle time.

AC CHARACTERISTICS

Symbol	Parameter	MIN	MAX	UNITS
F_{MAX}	Maximum input frequency (CLK)		100	MHz

Notes:

Maximum frequency of operation depends on Speed Grade. Check with ISI for availability.

THERMAL SPECIFICATIONS

Symbol	Parameter	MIN	MAX	UNITS
Θ_{JC}	Thermal resistance, junction to case		3.5	°C/W
Θ_{JB}	Thermal resistance, junction to board		8.6	°C/W